(1) Japanese Patent Application Laid-Open N . 58-124243 (1983) "Semiconductor Device Manufacturing Method"

The following is English translation of an extract from the above-identified document relevant to the present application.

The present invention allows a p+ type impurity layer 40 with a thickness thick enough for wiring to remain between a third oxide film 39 and a sapphire substrate 31. As a result, a semiconductor base 45 between source/drain regions 43 and 44 can be drawn out through the p+ type impurity layer 40 and a base drawing region 46 with law potential and further the potential can be fixed, thereby improving the circuit characteristics. Furthermore since the third oxide film 39 on the p+ type impurity layer 40 to become wiring is thick, stray capacitances between the wiring thereover and the silicon layer become small and circuit characteristics such as propagation speed will not be deteriorated.

The present invention is applicable not only to a semiconductor device with an SOS structure as described in the above embodiment but also to a case where a semiconductor element such as a three-dimensional circuit element is formed on a silicon layer on an SiO_2 film.